

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
11 October 2001 (11.10.2001)

PCT

(10) International Publication Number
WO 01/75956 A1

(51) International Patent Classification⁷: **H01L 21/316**

(21) International Application Number: **PCT/JP01/02262**

(22) International Filing Date: 22 March 2001 (22.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2000-95818 30 March 2000 (30.03.2000) JP

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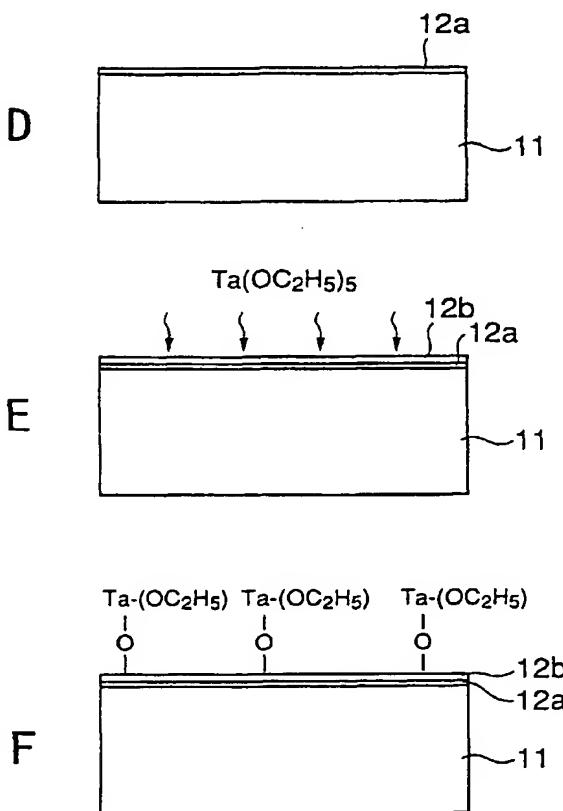
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[Continued on next page]

(54) Title: METHOD OF FORMING A DIELECTRIC FILM



(57) Abstract: A method of forming a dielectric film on a Si substrate comprises the steps of adsorbing a gaseous molecular compound of a metal element constituting a dielectric material on a Si substrate, and causing a decomposition of the gaseous molecular compound thus adsorbed by a hydrolysis process or pyrolytic decomposition process or an oxidation process.

WO 01/75956 A1

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(81) Designated States (*national*): KR, US.

(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION
METHOD OF FORMING A DIELECTRIC FILM

TECHNICAL FIELD

5 The present invention generally relates to semiconductor devices and more particularly to a fabrication process of ultrafine and ultrahigh-speed semiconductor devices.

10 BACKGROUND ART

With advancement in the art of device miniaturization, it is now becoming possible to use a gate length of 0.1 μm or less in leading-edge, ultrahigh-speed semiconductor devices. With increase 15 in the degree of device miniaturization, it is well known that there occurs an increase of the operational speed. On the other hand, in order to achieve such an increase of operational speed by way of device miniaturization, there is a requirement, 20 from scaling law, to reduce the thickness of a gate insulation film used therein in proportion with the reduction of a gate length of the semiconductor device.

In the case of ultrafine and ultrahigh-speed semiconductor devices having the gate length of 0.1 μm or less, it is thus necessary to reduce the thickness of the gate electrode to 1 - 2 nm or less, provided that SiO_2 is used for the material of the gate insulation film. However, the use of such an 30 extremely thin gate insulation film inevitably causes the problem of increase of leakage current caused by the tunneling effect through the thin gate insulation film.

Thus, in order to avoid the foregoing problem associated with the use of the SiO₂ film, there is proposed in Japanese Laid-Open Patent Publication 11-87341 a process of forming a thin SiN gate insulation film on the surface of a Si substrate in place of a SiO₂ gate insulation film, by first adsorbing a gaseous source material containing Si on the surface of the Si substrate, and then applying an atmosphere containing nitrogen radicals to the 5 substrate surface on which the gaseous source material is adsorbed. According to the foregoing proposal, the physical thickness of the gate insulation film can be increased while reducing the electrical or equivalent thickness of the gate 10 insulation film by using SiN, which has a larger specific dielectric constant than SiO₂, for the gate insulation film.

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This prior art process, however, is not effective for eliminating the foregoing problem of 20 tunneling leakage current. Although SiN has a specific dielectric constant of about 8, which is certainly larger than the specific constant of 4 for SiO₂, this value is not sufficient for achieving the desired increase of the physical thickness of the 25 gate insulation film while eliminating the tunneling current.

The process of the foregoing prior art has a further drawback, in relation to the use of the nitrogen radicals, in that it requires a plasma 30 process for exciting the nitrogen radicals. When the substrate surface is processed in the vicinity of a plasma source, charged particles forming the plasma such as electrons or ions are incorporated into the

SiN film and form impurity states therein. When such impurity states are formed in the gate insulation film, the leakage current in the gate insulation film is increased and the CV characteristic is degraded.

5 When the plasma source is provided at a remote location away from the substrate so as to avoid the foregoing problem, on the other hand, the number of the nitrogen radicals is reduced at the surface of the substrate and the adsorption of nitrogen becomes

10 difficult.

In view of the situation noted above, there is a proposal to use a high-dielectric material such as Ta₂O₅ for the material of the gate insulation film. It should be noted that these high-dielectric materials have a far larger specific dielectric constant as compared with SiO₂. By using such a high-dielectric material, it becomes possible to effectively reduce the equivalent thickness of the insulation film, which is an electrically equivalent thickness converted to the thickness of a SiO₂ film, while simultaneously using a large physical thickness. By using such a high-dielectric gate insulation film, it becomes possible to use a physical thickness of about 10 nm for the gate insulation film of ultrafine and ultrahigh-speed semiconductor devices having a gate length of 0.1 μ m or less, while successfully suppressing the gate leakage current caused by tunneling effect.

It has been known that a Ta₂O₅ film can be formed by a CVD process that uses Ta(OC₂H₅)₂ and O₂ as gaseous source. In a typical example, the CVD process is conducted under a reduced pressure environment at a temperature of 480°C or more. The Ta₂O₅ film thus

formed is then annealed in an oxidizing atmosphere for compensating for oxygen defects and for crystallization of the film. The Ta_2O_5 film thus crystallized shows a very large specific dielectric constant.

When growing a high-dielectric film such as Ta_2O_5 on a Si substrate by a CVD process, it is known that the growth of the high-dielectric film does not start immediately after the commencement of the CVD process due to a delay caused by nucleation process and that the growth starts only after a certain incubation time has elapsed.

In the experimental investigation that constitutes the foundation of the present invention, the inventor of the present invention has discovered that the incubation time varies depending on the nature of the layer on which the high-dielectric film is deposited. For example, the incubation time becomes very short when the deposition is made on a clean surface of a Si substrate from which oxide is removed. When there is an insulating film of SiO_2 or a SiN or $SiON$ on a Si substrate, on the other hand, a remarkable increase of the incubation time was observed. Further, it was discovered that the incubation time changes also depending on the thickness of the SiO_2 film or SiN film or the $SiON$ film existing on the surface of the Si substrate.

The foregoing discovery means that the thickness of the high-dielectric film formed on a SiO_2 film or on a SiN film or on a $SiON$ film on a Si substrate tends to reflect the variation of thickness of the underlying layer and that there may be a case in which the variation of the thickness of the

underlying layer may be amplified by the high-dielectric film. Further, the observed fact that the thickness of the high-dielectric film thus formed by a CVD process is affected by the nature of the 5 underlying layer indicates that the quality of the high-dielectric film thus formed for the gate insulation film may lack the desired homogeneity.

10 In order to suppress the occurrence of inhomogeneity in such high-dielectric film, it is necessary as well as desired to reduce the incubation time as much as possible.

15 Meanwhile, in such a semiconductor device that uses a high-dielectric film for the gate insulation film, it is necessary as well as desired to provide a thin oxide film between the Si substrate and the high-dielectric gate insulation film for 20 eliminating the diffusion of metal elements or impurity elements into the substrate forming the channel region of the semiconductor device from or through the high-dielectric film. Otherwise, there may be caused a problem of carrier scattering in the channel region by the metal elements.

25 On the other hand, such an intervening oxide film has to be extremely thin. When a thick oxide film is interposed between the Si substrate and the high-dielectric film, the effect of the high-dielectric film would be canceled out. In addition, there is a demand for a technology to change a film 30 quality such as composition in the thickness direction of the high-dielectric film.

DISCLOSURE OF THE INVENTION

Accordingly, it is a general object of the

present invention to provide a novel and useful method of forming a dielectric film wherein the foregoing problems are eliminated.

Another and more specific object of the 5 present invention is to provide a method of forming a dielectric film by a vapor phase deposition process without causing damages in the dielectric film by charged particles while minimizing the incubation time for deposition of the dielectric film and 10 simultaneously reducing the surface roughness.

Another object of the present invention is to provide a method of forming a dielectric film by a vapor phase deposition process without causing damages in the dielectric film by charged particles 15 while arbitrarily controlling a compositional profile of the dielectric film in a thickness direction thereof.

Another object of the present invention is to provide a method of forming a dielectric film on a 20 Si substrate, comprising the steps of:

exposing a surface of said Si substrate;
forming an insulating layer on said exposed surface of said Si substrate;
causing an adsorption of a gaseous 25 molecular compound of a metal element constituting a dielectric material at least once on said surface of said Si substrate on which said insulating layer has been formed, such that said gaseous molecular compound covers substantially uniformly over said 30 surface of said Si substrate; and
forming a molecular layer of said dielectric material containing said metal element on said surface of said Si substrate, by causing a

hydrolysis reaction in said gaseous molecular compound covering said surface of said Si substrate.

Another object of the present invention is to provide a method of forming a dielectric film on a 5 Si substrate, comprising the steps of:

exposing a surface of said Si substrate;

forming an insulating layer on said exposed surface of said Si substrate;

10 causing an adsorption of a gaseous molecular compound of a metal element constituting a dielectric material at least once on said insulating layer, such that said gaseous molecular compound covers substantially uniformly over said insulating layer; and

15 forming a molecular layer of said dielectric material containing said metal element on said insulating layer, by causing a pyrolytic decomposition of said gaseous molecular compound covering said insulating layer,

20 said step of causing a pyrolytic decomposition comprising the step of heating said Si substrate to a temperature exceeding a pyrolytic decomposition temperature of said gaseous molecular compound in an oxidizing atmosphere.

25 Another object of the present invention is to provide a method of forming a dielectric film on a Si substrate, comprising the steps of:

exposing a surface of said Si substrate;

30 forming an insulating layer on said exposed surface of said Si substrate;

causing an adsorption of a gaseous molecular compound of a metal element constituting a dielectric material at least once on said insulating

layer, such that said gaseous molecular compound covers substantially uniformly over said insulating layer; and

5 forming a molecular layer of said dielectric material containing said metal element on said insulating layer, by exposing said gaseous molecular compound to an atmosphere selected from the group consisting of H_2O , O_3 and NO_2 .

According to the present invention, it 10 becomes possible to form a dielectric or high-dielectric film of various compositions including Ta_2O_5 on a Si substrate by a CVD process with reduced incubation time. As a result, the uniformity of the obtained dielectric film is improved. Further, the 15 present invention enables arbitrary control of composition of the dielectric film in the thickness direction thereof. According to the needs, it is also possible to form an extremely thin diffusion barrier film of about a single molecular layer thickness 20 inside the dielectric film. In view of the fact that the present invention does not include the step of using plasma-excited radials, the dielectric film thus formed according to the process of the present invention is substantially free from defects having 25 electric charges such as impurity states, and excellent leakage characteristics can be attained.

As a result of the present invention, a ultrafine and ultrahigh-speed semiconductor device having a gate length of $0.1 \mu m$ or less can be formed 30 while successfully suppressing the gate leakage current.

Other objects and further features of the present invention will become apparent from the

following detailed description when read in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

5 FIGS.1A - 1H are diagrams showing the process of forming a dielectric film according to a first embodiment of the present invention;

FIG.2 is a diagram showing the effect of the present invention;

10 FIGS.3A and 3B are diagrams showing a surface structure of a Ta₂O₅ film formed on a SiON film according to a conventional CVD process;

15 FIGS.4A and 4B are diagrams respectively showing the surface structure of a Ta₂O₅ film formed on a SiON substrate according to a process of the present invention and the surface structure of a Ta₂O₅ film formed directly on a Si substrate surface;

20 FIG.5 is a diagram showing the process conditions used in the present embodiment and in various modifications thereof;

FIG.6 is a further diagram showing the process conditions used in the present embodiment and in various modifications thereof;

25 FIG.7 is a flowchart showing the process of forming a dielectric film according to a second embodiment of the present invention;

FIG.8 is a diagram showing the structure of a dielectric film formed according to the second embodiment of the present invention;

30 FIG.9 is a diagram showing the structure of a dielectric film formed according to a third embodiment of the present invention; and

FIG.10 is a diagram showing the

construction of a semiconductor device according to a fourth embodiment of the present invention.

BEST MODE OF IMPLEMENTING THE INVENTION

5 [FIRST EMBODIMENT]

FIGS.1A - 1H show the process of forming a Ta₂O₅ film according to a first embodiment of the present invention.

Referring to FIG.1A, a Si substrate 11 is held in a reaction vessel (not shown) under a reduced pressure environment of 133 - 399 Pa (1 - 3 Torr) at a temperature lower than a room temperature, and an oxide film 11a on the surface of the substrate 11 is removed by supplying nitrogen radicals N* and hydrogen radicals H* formed as a result of plasma activation of a gas mixture of N₂ and H₂ into the reaction vessel together with a NF₃ gas. By conducting such a removal of the oxide film at low temperature, there is formed a protective film 11b having a composition of N-O-Si-H on the surface of the Si substrate 11. In a typical example, the H₂ gas, the NF₃ gas and the N₂ gas are supplied with respective flow rates of 10 sccm, 30 sccm and 100 sccm, and the activation of the H₂ gas and the N₂ gas is achieved by applying a plasma power of about 50W. The process of FIG.1A may be continued for a duration of 3 minutes or less.

The protective film 11b thus formed is a volatile film and easily undergoes vaporization by causing sublimation in the step of FIG.1C when the Si substrate 11 is annealed subsequently to the step of FIG.1B in the same reaction vessel under the reduced pressure environment at a temperature of about 120° C.

As a result a fresh surface 11c of the Si substrate 11 is exposed.

Next, in the step of FIG.1D, which is continued from the step of FIG.1C, the pressure 5 inside the reaction vessel is set to 1.33 - 13.3 Pa (0.01 - 0.1 Torr) and the substrate temperature is set to 200 - 350 °C. In this state, a SiCl₄ gas is introduced into the reaction vessel with a flow rate of 0.1 - 5 mg/min together with a He carrier gas, 10 which is supplied to the reaction vessel with a flow rate of about 50 sccm. In this step, SiCl₄ molecules thus introduced with the SiCl₄ gas cause adsorption on the foregoing fresh surface 11c of the Si substrate 11.

15 In the step of FIG.1D, an H₂O vapor is then introduced into the reaction vessel with a flow rate of about 1 sccm together with the He carrier gas, wherein the H₂O vapor thus introduced causes a hydrolysis reaction in the SiCl₄ molecules absorbed 20 on the surface 11c of the Si substrate 11. As a result, there is formed an extremely thin SiO₂ molecular layer 12a containing one to several layers of SiO₂ molecules on the surface of the Si substrate 11. By repeating the process of introducing the SiCl₄ 25 gas and the process of hydrolysis of the absorbed SiCl₄ molecules in the step of FIG.1D, it is possible to form the SiO₂ molecular layer 12a to have a desired thickness.

In the step of FIG.1D, it is also possible 30 to use a SiH₂Cl₂ gas or a Si(C₂H₅)₅ gas in place of the SiCl₄ gas.

In the step of FIG.1D, it should also be noted that the SiO₂ molecular layer 12a may be

replaced by a SiN molecular layer by processing the adsorbed SiCl₄ molecules by a NH₃ gas. Further, it is possible to form an SiON molecular layer by stacking the SiO₂ molecular layer and the SiN molecular layer 5 as desired. Further, it is also possible to form a thermal oxide film in view of availability of abundant data for process control.

Next, in the step of FIG.1E, the substrate temperature is set to 350° C or less, preferably about 10 300° C or less, most preferably to about 280° C, and a Ta(OC₂H₅)₅ gas and an O₂ gas are supplied to the reaction vessel held at a pressure of 0.01 - 0.1 Torr similarly as before, together with a He carrier gas with respective flow rates of about 5 mg/min and 100 15 sccm for about 1 minute. The flow rate of the He carrier gas is set to about 100 sccm. As a result, the Ta(OC₂H₅)₅ molecules are adsorbed on the SiO₂ layer 12a in the form of a Ta(OC₂H₅)₅ molecular layer 12b.

20 Next, in the step of FIG.1G, the substrate temperature is raised to about 350° C in an oxidizing atmosphere and oxidation or hydrolysis reaction is caused in the adsorbed Ta(OC₂H₅)₅ molecules. As a result, the adsorbed molecular layer 12b of 25 Ta(OC₂H₅)O₅ is converted into a Ta₂O₅ molecular layer 12c.

Further, in the step of FIG.1H, the substrate temperature is raised to 510° C and the internal pressure of the reaction vessel is set to 30 13.3 - 1330 Pa (0.1 - 10 Torr). Further, the Ta(OC₂H₅)₅ gas and the O₂ gas are introduced into the reaction vessel together with the He carrier gas and a Ta₂O₅ film 13 is formed on the Ta₂O₅ molecular layer

12c by an ordinary CVD process with a thickness of 4 - 5 nm.

While not illustrated, the Ta₂O₅ film 13 is subjected to a thermal annealing process conducted in an O₂ atmosphere for compensation of oxygen defects and crystallization. The Ta₂O₅ film 13 thus crystallized shows a large specific dielectric constant. In view of the fact that the SiO₂ molecular layer 12a is interposed at the interface between the Si substrate 11 and the Ta₂O₅ film 13, a large carrier mobility is guaranteed for the semiconductor device formed on the Si substrate. In other words, the semiconductor device formed according to the present invention operates at a very high speed.

FIG.2 shows the relationship between the duration of the deposition process in the CVD step of FIG.1H and the thickness of the Ta₂O₅ film 13 thus formed, in comparison with a conventional CVD process of a Ta₂O₅ film. In FIG.2, it should be noted that the deposition time is measured from the point of commencement of the CVD process. In FIG.2, ● represents the deposition of the Ta₂O₅ film according to the present embodiment, while ▲ represents the deposition of the Ta₂O₅ film according to the conventional CVD process. In the conventional experiments represented by ▲, it should be noted that the CVD deposition of the Ta₂O₅ film is conducted directly on the SiO₂ molecular layer 12a.

Referring to FIG.2, it can be seen that there exists an incubation time of about 140 seconds from the start of the CVD process until actual deposition of the Ta₂O₅ film is caused, while in the case of the present invention, the deposition of the

Ta₂O₅ film is already started after 40 seconds from the commencement of the CVD process. Thus, the present invention can substantially reduce the incubation time at the time of forming a Ta₂O₅ film by a CVD process.

FIGS.3A and 3B show the result of an AFM (atomic-force microscope) observation of the surface of the Ta₂O₅ film formed on a SiON film covering the surface of the Si substrate by a conventional CVD process, wherein FIG.3A represents the case in which the CVD process of the Ta₂O₅ film is conducted at the substrate temperature of 510° C, while FIG.3B represents the case in which the CVD process of the Ta₂O₅ film is conducted at the substrate temperature of 480° C.

Referring to FIGS.3A and 3B, the CVD-Ta₂O₅ film thus formed has a very large variation of film thickness reflecting the variation of the film thickness of the underlying SiON film. In other words, there occurs an amplification of thickness variation of the underlying layer in the conventional CVD-Ta₂O₅ film and the homogeneity of the obtained Ta₂O₅ film becomes inevitably deteriorated.

FIG.4A, on the other hand, shows the surface of the Ta₂O₅ film formed according to the present embodiment explained with reference to FIGS.1A - 1H, wherein it should be noted that the Ta₂O₅ film is formed not on the SiO₂ molecular layer 12a but on an SiON molecular layer. FIG.4B, on the other hand, shows the surface of the Ta₂O₅ film deposited directly on the exposed surface 11c of the Si substrate 11. In any of FIGS.4A and 4B, the surface structure of the Ta₂O₅ film was observed by

an AFM.

Referring to FIG.4A, it can be seen that the projections and depressions on the Ta₂O₅ film formed by the CVD process is reduced substantially by 5 employing the process of the present invention. In other words, FIG.4A indicates that it is possible to obtain a Ta₂O₅ film having a surface similar to that of the film formed directly on a Si substrate by employing the process of the present invention. It is 10 believed that this advantageous result of FIG.4A reflects the decrease of the incubation time achieved as a result of conducting the CVD process of the Ta₂O₅ film 13 on the Ta₂O₅ molecular layer 12c, which in turn is formed as a result of oxidation of the 15 gaseous molecular compound Ta(OC₂H₅)₅ adsorbed on the underlying SiON film layer, as explained with reference to FIG.2. As a result of the decrease of the incubation time depending on the quality of the underlying film, the variation of the incubation time 20 itself is reduced, and the variation of the thickness of the Ta₂O₅ film 13 thus formed by the CVD process is also reduced.

In the present invention, it should be noted that the gaseous molecular compound usable for 25 forming the Ta₂O₅ molecular layer 12c is not limited to Ta(OC₂H₅)₅ but it is also possible to use TaCl₅. When TaCl₅ is used, the adsorption process may be conducted by setting the internal pressure of the reaction vessel to 0.133 - 13.3 Pa (0.001 - 00.1 30 Torr) and by supplying the TaCl₅ gas with a flow rate of 0.1 - 5 mg/min while maintaining the substrate temperature of 200 - 300°C.

Further, the present invention is not

limited to the process of forming a Ta_2O_5 film but may be applicable also for forming various oxide films including a SiO_2 film, a ZrO_2 film, a HfO_2 film or an Al_2O_3 film as summarized in FIGS.5 and 6.

5 wherein it should be noted that FIG.5 summarizes the process condition for the adsorption process and oxidizing process corresponding respectively to the steps of FIGS.1F and 1G; for the foregoing oxides, while FIG.6 summarizes the process condition for the

10 CVD process corresponding to the step of FIG.1H.

Referring to FIG.5, it can be seen that the atmosphere used for oxidizing or causing hydrolysis reaction in the step of FIG.1F for forming the Ta_2O_5 molecular layer 12c from the adsorbed $Ta(OC_2H_5)_5$ molecules or $TaCl_2$ molecules is not limited to the O_2 atmosphere, but other oxidizing atmospheres including a H_2O atmosphere, a NO_2 atmosphere or an O_3 atmosphere may also be used. In the event the oxidizing atmosphere of FIG.1G is conducted in the O_2 atmosphere as explained before, it is preferable to set the internal pressure of the reaction vessel to 0.133 - 1330 Pa (0.01 - 10 Torr) and the substrate temperature of 300 - 400°C. In the event the oxidizing step of FIG.1F is to be conducted in the O_3 atmosphere, on the other hand, it is preferable to set the internal pressure of the reaction vessel to 0.133 - 1330 Pa (0.001 - 10 Torr) and the substrate temperature to 200 - 300°C.

As can be seen in FIG.5, it is also possible to form a ZrO_2 molecular layer in place of the Ta_2O_5 molecular layer 12c by adsorbing a gaseous molecular compound of Zr such as $Zr(t-OC_4H_9)_4$ or $ZrCl_4$ on the SiO_2 molecular layer 12a in the step of FIG.1F

and oxidizing the same under a similar condition as in the case of using the Ta gaseous molecular compound in the step of FIG.1F. Similarly, it is also possible to form a HfO₂ molecular layer by adsorbing 5 a gaseous molecular compound of Hf such as Hf(t-OC₄H₉)₄ or HfCl₄ on the SiO₂ molecular layer 12a and oxidizing the same under a similar condition as in the case of forming the Ta₂O₅ molecular layer. Further, it is possible to form an Al₂O₃ molecular 10 layer in place of the Ta₂O₅ molecular layer 12c by adsorbing a gaseous molecular compound of Al such as Al(l-OC₃H₇)₃ or (CH₃)₃Al on the SiO₂ molecular layer 12a and oxidizing the same under a similar condition as in the case of forming the Ta₂O₅ molecular layer. 15 It is also possible to form the molecular layer 12c from SiO₂ by adsorbing Si(OC₂H₅)₄ or SiCl₄ or SiH₂Cl₂ on the SiO₂ molecular layer 12a under the condition similar to that of the Ta₂O₅ molecular layer and further causing oxidation or hydrolysis in 20 the gaseous molecular compound of Si thus absorbed under a similar condition.

Further, by conducting a CVD process on the oxide molecular layer 12c thus formed under the condition summarized in FIG.6, it becomes possible to 25 form a CVD film of various oxides including Ta₂O₅, ZrO₂, HfO₂, SiO₂ and Al₂O₃ as the CVD film 13.

[SECOND EMBODIMENT]

FIG.7 shows the process of forming a 30 dielectric film according to a second embodiment of the present invention in the form of flowchart.

Referring to FIG.7, the gaseous molecules of SiCl₄ are adsorbed on the SiO₂ molecular layer 12a

represented in FIG.1D in the step S1, and the SiCl₄ molecules thus adsorbed are subjected to an oxidation or hydrolysis reaction in the step S2. As a result, there is formed a molecular layer of SiO₂ on the 5 substrate 11.

The foregoing steps S1 and S2 are repeated alternately a predetermined times X in the next step S3, and the process proceeds further to the step S4 corresponding to the process steps of FIGS.1E and 1F 10 in which the molecules of ZrCl₄ or Zr(t-OC₄H₉)₄ are adsorbed on the SiO₂ molecular layer formed in the previous steps S1 and S2.

The gaseous molecular compound of Zr thus adsorbed are then subjected to an oxidation or 15 hydrolysis reaction in the next step S5 corresponding to the process step of FIG.1G, and there is formed a molecular layer of ZrO₂ on the SiO₂ molecular layer. Further, the foregoing steps S4 and S5 are repeated alternately Y times in the next step S6, and the 20 number of repetition X and Y are changed to X1 and Y1 respectively in the next step S7.

After the step S7, the process returns to the step S1. Thus, by repeating the steps S1 - S7 with the newly defined number of the repetition X1 25 and Y1, there is formed a dielectric film having a composition of ZrSiO₄ on the Si substrate in such a manner that the proportion of Zr and Si changes continuously in the thickness direction of the layer as represented in FIG.8, wherein FIG.8 represents 30 those parts corresponding to the parts described previously by corresponding reference numerals.

Referring to FIG.8, it can be seen that the Zr content in the dielectric film is controlled such

that the Zr content is small in the vicinity of the interface to the Si substrate 11 and increases with increasing distance from the foregoing interface. In the $ZrSiO_4$ film having such a compositional profile, 5 there is an advantageous feature, associated with the increased Si content in the vicinity of the interface to the Si substrate, of improved adherence. Further, in view of the fact that the large Zr content in the vicinity of the surface of the $ZrSiO_4$ film, the 10 leakage current through the dielectric film is suppressed effectively. Further, it is possible to form the $ZrSiO_4$ film such that a Zr atom and a Si atom are repeated alternately in the thickness direction in every one molecular layer in the $ZrSiO_4$ 15 film.

[THIRD EMBODIMENT]

FIG.9 shows the structure of a dielectric film according to a third embodiment of the present invention, wherein those parts corresponding to the parts described previously are designated by the same reference numerals and the description thereof will be omitted.

Referring to FIG.9, the present embodiment 25 carries out adsorption of $SiCl_4$ molecules on the SiO_2 molecular layer 12a and the $SiCl_4$ molecules are converted to a molecular layer 12d of SiN by processing the adsorbed $SiCl_4$ molecules by an NH_3 gas. After the formation of the SiN molecular layer 12d, 30 the $Ta(OC_2H_5)_5$ molecules are adsorbed on the layer 12d, and are converted to the Ta_2O_5 molecular layer 12c as a result of oxidation. Further, the CVD- Ta_2O_5 layer 13 is formed on the Ta_2O_5 molecular layer 12c.

In the structure of FIG.9, it is possible to eliminate the problem of diffusion of B into the Si substrate by the SiN molecular layer 12d when a B-doped polysilicon film is deposited on the Ta₂O₅ film 13. It should be noted that the SiN molecular layer 12d interposed between the Ta₂O₅ film 13 and the Si substrate 11 effectively blocks the diffusion of B. Thus, the structure of FIG.9 is effective for eliminating the variation of the threshold characteristic

[FOURTH EMBODIMENT]

FIG.10 shows the construction of a semiconductor device according to a fourth embodiment 15 of the present invention.

Referring to FIG.10, there is formed a gate insulation film 22 of Ta₂O₅ on a p-type substrate according to a process described in any of the preceding embodiments, and a polysilicon gate 20 electrode 23 is formed on the gate insulation film 22.

Further, the Si substrate 21 is formed with diffusion regions 21A and 21B of n⁻-type adjacent to the gate electrode 23, and sidewall insulation films 23a and 23b are provided on respective sidewalls of 25 the polysilicon gate electrode 23. Further, diffusion regions 21C and 21D of n⁺-type are formed outside of the sidewall insulation films 23a and 23b respectively.

In the semiconductor device of FIG.10, an 30 effective film thickness electrically equivalent to a SiO₂ film having a thickness of 0.1 nm or less is realized by using Ta₂O₅ for the gate insulation film 22, and a ultrahigh-speed operation is achieved by

reducing the gate length while simultaneously suppressing the gate leakage current. By forming the Ta₂O₅ film 22 according to the process described in any of the preceding embodiments, it becomes possible 5 to minimize the variation of the film thickness and the semiconductor device thus formed has reliable and reproducible characteristics. Particularly, it is possible to block the diffusion of the impurity element from the gate electrode 12 to the Si 10 substrate 21 by intervening a molecular layer 12d of SiN right underneath the Ta₂O₅ film 22 with a thickness of several molecular layers.

By forming the gate insulation film 22 in the form of stacking of molecular layers of various 15 oxides including Ta₂O₅, it is possible to control the compositional profile inside the gate insulation film 22 in the thickness direction thereof as desired. As a result, a structure having excellent adhesion to the Si substrate can be formed easily for the gate 20 insulation film, such that the gate insulation film has a large specific dielectric constant at the interface to the gate electrode 23.

As the forgoing process of forming the dielectric molecular film on the substrate is 25 achieved by a hydrolysis reaction of the adsorbed gaseous source molecules in the present invention contrary to the conventional process of the Japanese Laid-Open Patent Publication 11-97341, which uses plasma-excited radicals, it becomes possible to avoid 30 the problem pertinent to the foregoing prior art of the charged particles incorporated into the dielectric film forming a leakage current path, is successfully avoided. As there occur only thermally

stable reactions in the hydrolysis process, the control of such a hydrolysis reaction is made easily.

Further, the present invention is not limited to the embodiments described heretofore, but 5 various variations and modifications may be made without departing from the scope of the invention.

INDUSTRIAL APPLICABILITY

According to the present invention, it 10 becomes possible to form a dielectric or high-dielectric film of various compositions including Ta_2O_5 on a Si substrate by a CVD process with reduced incubation time. As a result, the uniformity of the obtained dielectric film is improved. Further, the 15 present invention enables arbitrary control of composition of the dielectric film in the thickness direction thereof. According to the needs, it is also possible to form an extremely thin diffusion barrier film of about a single molecular layer thickness in 20 the dielectric film. In view of the fact that the present invention does not include the step of using plasma-excited radials, the dielectric film thus formed according to the process of the present invention is substantially free from defects having 25 electric charges such as impurity states, and excellent leakage characteristics can be attained. As a result of the present invention, a ultrafine and ultrahigh-speed semiconductor device having a gate length of 0.1 μm or less can be formed while 30 successfully suppressing the gate leakage current.

CLAIMS

5

1. A method of forming a dielectric film on a Si substrate, comprising the steps of:

exposing a surface of said Si substrate;

10 forming an insulating layer on said exposed surface of said Si substrate;

causing an adsorption of a gaseous molecular compound of a metal element constituting a dielectric material at least once on a surface of said insulating layer, such that said gaseous

15 molecular compound covers substantially uniformly over said insulating layer; and

forming a molecular layer of said dielectric material containing said metal element on said insulating layer, by causing a hydrolysis of

20 said gaseous molecular compound covering said insulating layer.

25

2. A method as claimed in claim 1, wherein said dielectric material comprises Ta_2O_5 and wherein said gaseous molecular compound comprises any of $Ta(OC_2H_5)_5$ and $TaCl_5$.

30

24

3. A method as claimed in claim 1, wherein
said dielectric material comprises ZrO_2 and wherein
said gaseous molecular compound comprises any of
 $Zr(t-OC_4H_9)_4$ and $ZrCl_4$.

5

4. A method as claimed in claim 1, wherein
10 said dielectric material comprises HfO_2 and wherein
said gaseous molecular compound comprises any of
 $Hf(t-OC_4H_9)_4$ and $HfCl_4$.

15

5. A method as claimed in claim 1, wherein
said dielectric material comprises Al_2O_3 and wherein
said gaseous molecular compound comprises any of
20 $Al(l-OC_3H_7)_3$ and $(CH_3)_3Al$.

25

6. A method as claimed in claim 1, wherein
said step of forming said insulating layer comprises
the steps of: covering said exposed surface of said
Si substrate substantially uniformly by a gaseous
molecular compound of Si at least once, by adsorbing
30 said gaseous molecular compound of Si on said exposed
surface of said Si substrate; and causing a
hydrolysis of said gaseous molecular compound of Si,
said gaseous molecular compound of Si being selected

from the group consisting of SiCl_4 , SiH_2Cl_2 and $\text{Si}(\text{C}_2\text{H}_5)_5$.

5

7. A method as claimed in claim 1, wherein said step of forming said insulating layer on said Si substrate comprises the step of applying a thermal 10 oxidation process to said exposed surface of said Si substrate.

15

8. A method as claimed in claim 1 further comprising the step of forming, after said step of hydrolysis, a high-dielectric film on said molecular layer of said dielectric material by a CVD process.

20

9. A method as claimed in claim 1, wherein 25 said step of forming said molecular layer of said dielectric material comprises the step of forming a dielectric film having a composition represented as ZrSiO_4 , such that said dielectric film has a low Zr concentration level at an interface to said Si substrate and such that said Zr concentration level 30 increases with increasing distance from said interface.

10. A method as claimed in claim 9, wherein
said step of forming said dielectric film comprises
the steps of forming a SiO_2 molecular layer and a
 ZrO_2 molecular layer consecutively, said step of
5 forming said SiO_2 molecular layer comprising the
steps of: adsorbing molecules of a first gaseous
source material containing Si on an underlying layer;
and decomposing said adsorbed molecules of said first
gaseous source material, said step of forming said
10 ZrO_2 molecular layer comprising the steps of:
adsorbing molecules of a second gaseous source
material containing Zr on an underlying layer; and
decomposing said adsorbed molecules of said second
gaseous source material.

15

11. A method of forming a dielectric film
20 on a Si substrate, comprising the steps of:
exposing a surface of said Si substrate;
forming an insulating layer on said exposed
surface of said Si substrate;
causing an adsorption of a gaseous
25 molecular compound of a metal element constituting a
dielectric material at least once on said insulating
layer, such that said gaseous molecular compound
covers substantially uniformly over said insulating
layer; and
30 forming a molecular layer of said
dielectric material containing said metal element on
said insulating layer, by causing a pyrolytic
decomposition of said gaseous molecular compound

covering said insulating layer,
said step of causing a pyrolytic
decomposition comprising the step of heating said Si
substrate to a temperature exceeding a pyrolytic
5 decomposition temperature of said gaseous molecular
compound in an oxidizing atmosphere.

10

12. A method as claimed in claim 11,
wherein said dielectric material comprises Ta_2O_5 and
wherein said gaseous molecular compound comprises any
of $Ta(OC_2H_5)_5$ and $TaCl_5$.

15

13. A method as claimed in claim 11,
20 wherein said dielectric material comprises ZrO_2 and
wherein said gaseous molecular compound comprises any
of $Zr(t-OC_4H_9)_4$ and $ZrCl_4$.

25

14. A method as claimed in claim 11,
wherein said dielectric material comprises HfO_2 and
wherein said gaseous molecular compound comprises any
30 of $Hf(t-OC_4H_9)_4$ and $HfCl_4$.

15. A method as claimed in claim 11,
wherein said dielectric material comprises Al_2O_3 and
wherein said gaseous molecular compound comprises any
of $Al(1-OC_3H_7)_3$ and $(CH_3)_3Al$.

5

16. A method as claimed in claim 11,
10 wherein said step of forming said insulating layer
comprises the steps of: covering said exposed surface
of said Si substrate substantially uniformly by a
gaseous molecular compound of Si at least once, by
adsorbing said gaseous molecular compound of Si on
15 said exposed surface of said Si substrate; and
causing a hydrolysis of said gaseous molecular
compound of Si, said gaseous molecular compound of Si
being selected from the group consisting of $SiCl_4$,
 SiH_2Cl_2 and $Si(C_2H_5)_5$.

20

17. A method as claimed in claim 11,
25 wherein said step of forming said insulating layer on
said Si substrate comprises the step of applying a
thermal oxidation process to said exposed surface of
said Si substrate.

30

18. A method as claimed in claim 11 further

comprising the step of forming, after said step of pyrolytic decomposition, a high-dielectric film on said molecular layer of said dielectric material by a CVD process.

5

19. A method as claimed in claim 11,
10 wherein said step of forming said molecular layer of said dielectric material comprises the step of forming a dielectric film having a composition represented as $ZrSiO_4$, such that said dielectric film has a low Zr concentration level at an interface to
15 said Si substrate and such that said Zr concentration level increases with increasing distance from said interface.

20

20. A method as claimed in claim 19,
wherein said step of forming said dielectric film comprises the steps of forming a SiO_2 molecular layer
25 and a ZrO_2 molecular layer consecutively, said step of forming said SiO_2 molecular layer comprising the steps of: adsorbing molecules of a first gaseous source material containing Si on an underlying layer; and decomposing said adsorbed molecules of said first gaseous source material, said step of forming said
30 ZrO_2 molecular layer comprising the steps of: adsorbing molecules of a second gaseous source material containing Zr on an underlying layer; and

decomposing said adsorbed molecules of said second gaseous source material.

5

21. A method of forming a dielectric film on a Si substrate, comprising the steps of:

10 exposing a surface of said Si substrate; forming an insulating layer on said exposed surface of said Si substrate;

15 causing an adsorption of a gaseous molecular compound of a metal element constituting a dielectric material at least once on said insulating layer, such that said gaseous molecular compound covers substantially uniformly over said insulating layer; and

20 forming a molecular layer of said dielectric material containing said metal element on said insulating layer, by exposing said gaseous molecular compound to an atmosphere selected from the group consisting of H_2O , O_3 and NO_2 .

25

22. A method as claimed in claim 21, wherein said dielectric material comprises Ta_2O_5 and wherein said gaseous molecular compound comprises any 30 of $Ta(OC_2H_5)_5$ and $TaCl_5$.

23. A method as claimed in claim 21,
wherein said dielectric material comprises ZrO_2 and
wherein said gaseous molecular compound comprises any
5 of $Zr(t-OC_4H_9)_4$ and $ZrCl_4$.

10 24. A method as claimed in claim 21,
wherein said dielectric material comprises HfO_2 and
wherein said gaseous molecular compound comprises any
of $Hf(t-OC_4H_9)_4$ and $HfCl_4$.

15

25. A method as claimed in claim 21,
wherein said dielectric material comprises Al_2O_3 and
20 wherein said gaseous molecular compound comprises any
of $Al(l-OC_3H_7)_3$ and $(CH_3)_3Al$.

25

26. A method as claimed in claim 21,
wherein said step of forming said insulating layer
comprises the steps of: covering said exposed surface
of said Si substrate substantially uniformly by a
30 gaseous molecular compound of Si at least once, by
adsorbing said gaseous molecular compound of Si on
said exposed surface of said Si substrate; and
causing a hydrolysis of said gaseous molecular

compound of Si, said gaseous molecular compound of Si being selected from the group consisting of SiCl_4 , SiH_2Cl_2 and $\text{Si}(\text{C}_2\text{H}_5)_5$.

5

27. A method as claimed in claim 21, wherein said step of forming said insulating layer on said Si substrate comprises the step of applying a thermal oxidation process to said exposed surface of said Si substrate.

15

28. A method as claimed in claim 21 further comprising the step of forming, after said step of exposure to said atmosphere, a high-dielectric film on said molecular layer of said dielectric material by a CVD process.

25

29. A method as claimed in claim 21, wherein said step of forming said molecular layer of said dielectric material comprises the step of forming a dielectric film having a composition represented as ZrSiO_4 , such that said dielectric film has a low Zr concentration level at an interface to said Si substrate and such that said Zr concentration level increases with increasing distance from said

interface.

5

30. A method as claimed in claim 29,
wherein said step of forming said dielectric film
comprises the steps of forming a SiO_2 molecular layer
and a ZrO_2 molecular layer consecutively, said step
10 of forming said SiO_2 molecular layer comprising the
steps of: adsorbing molecules of a first gaseous
source material containing Si on an underlying layer;
and decomposing said adsorbed molecules of said first
gaseous source material, said step of forming said
15 ZrO_2 molecular layer comprising the steps of:
adsorbing molecules of a second gaseous source
material containing Zr on an underlying layer; and
decomposing said adsorbed molecules of said second
gaseous source material.

20

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FIG. 1A

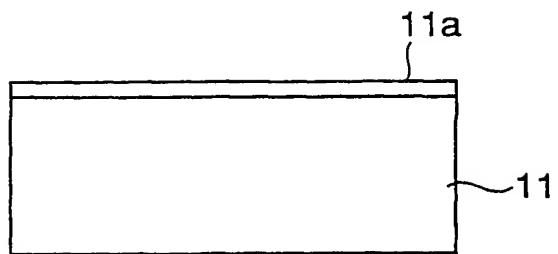


FIG. 1B

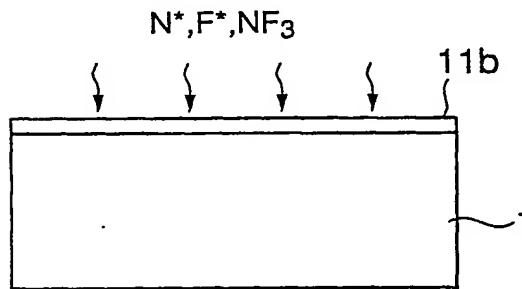
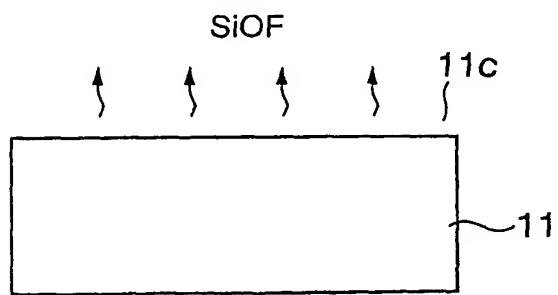


FIG. 1C



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FIG. 1D

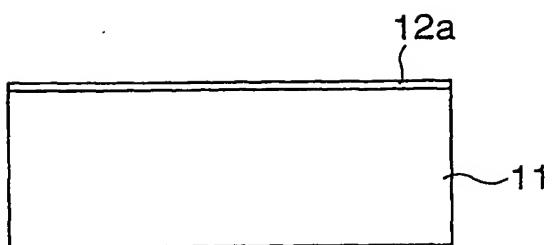


FIG. 1E

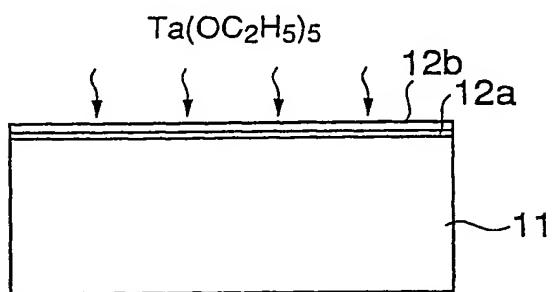
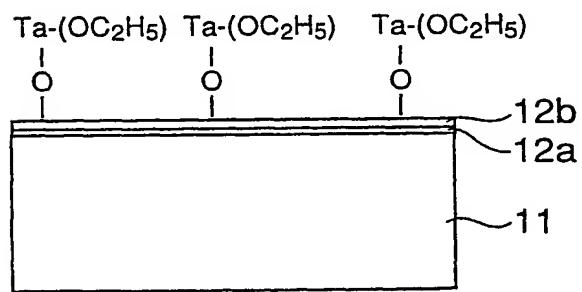


FIG. 1F



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FIG. 1G

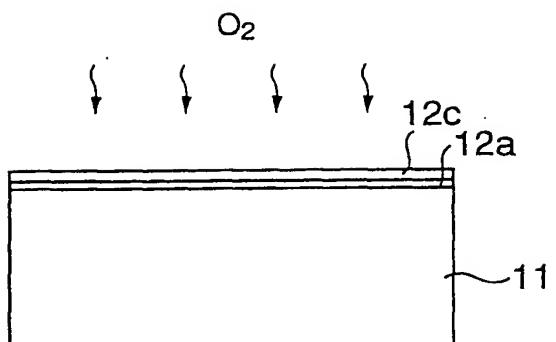
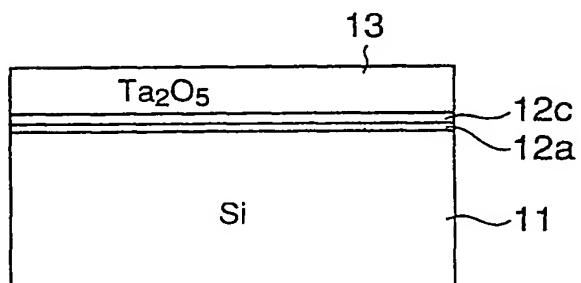


FIG. 1H



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FIG. 2

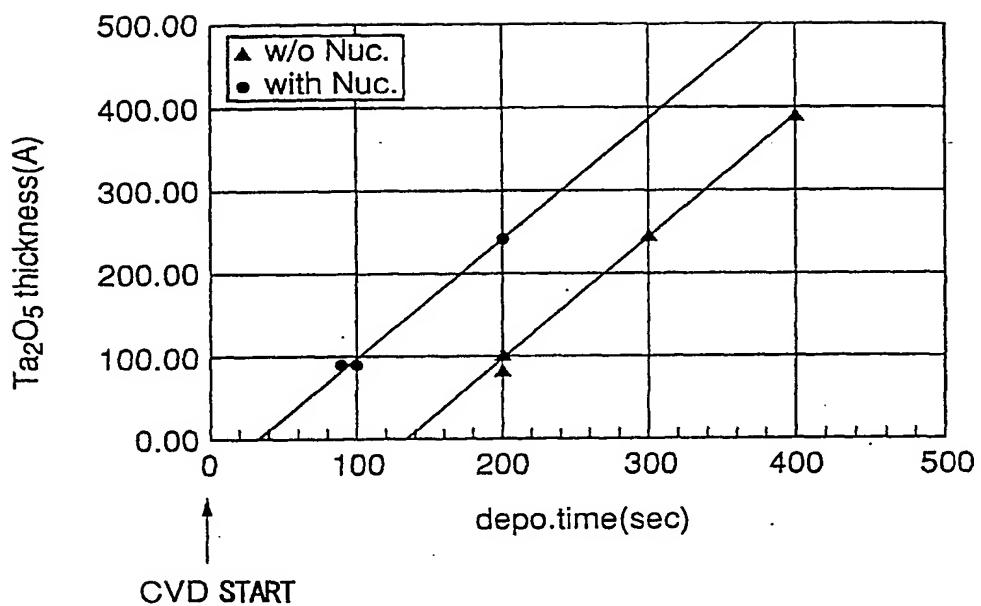


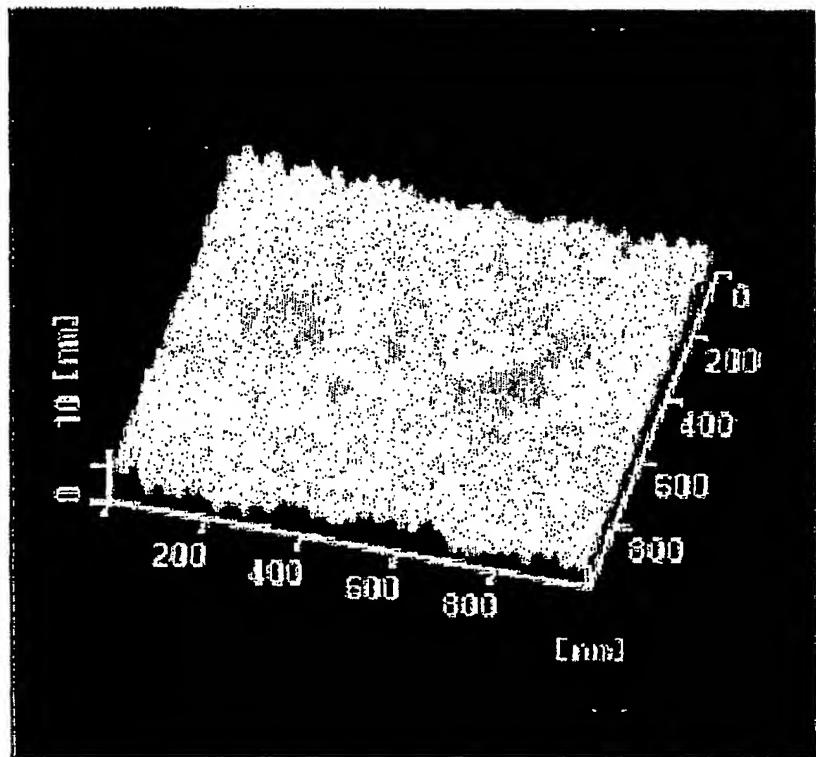
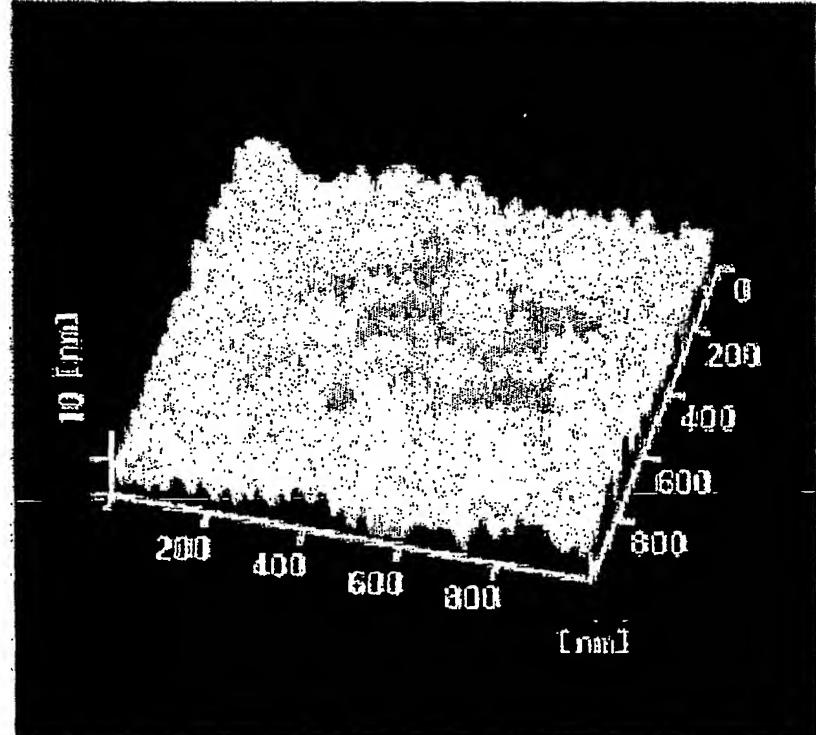
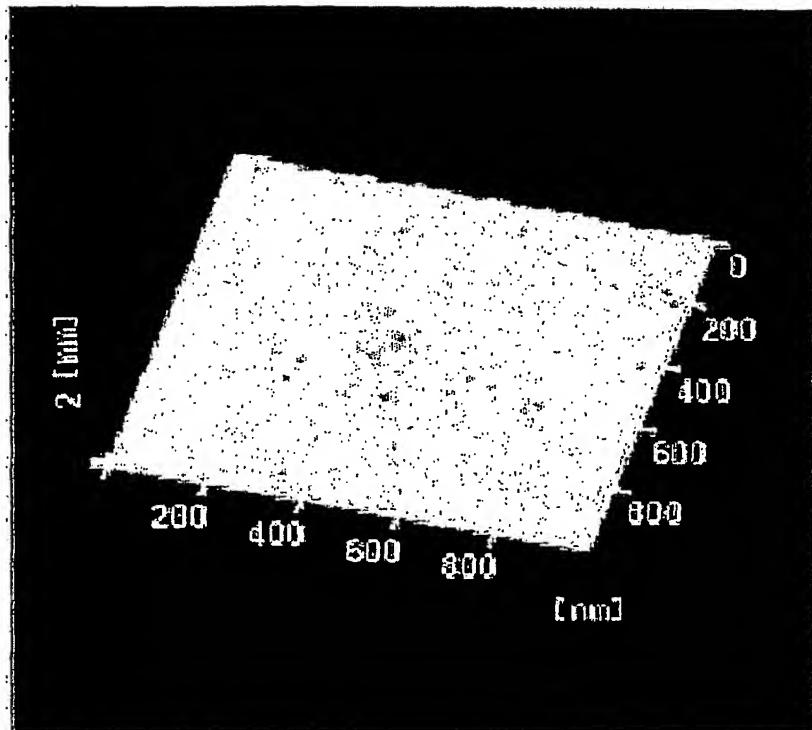
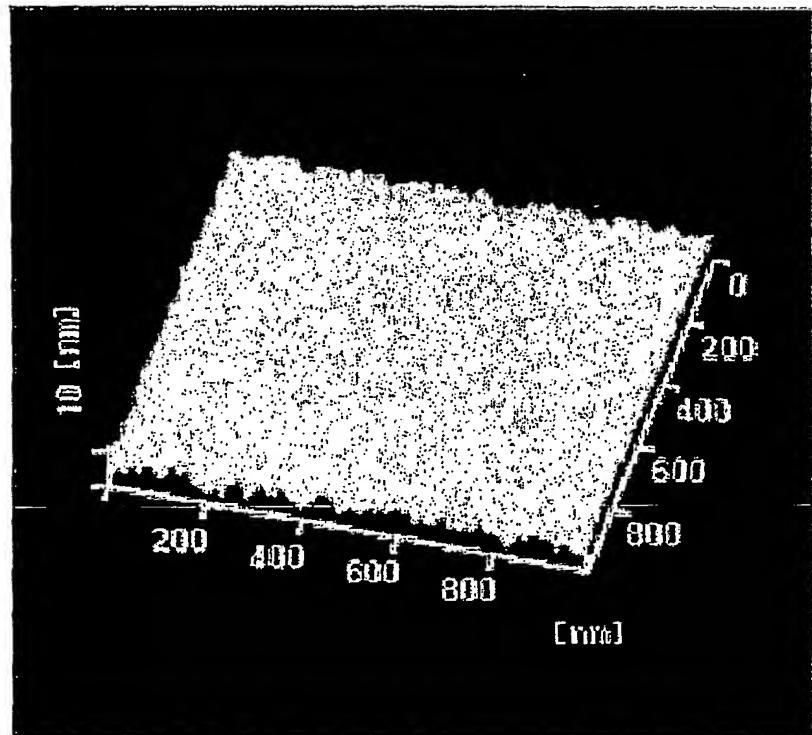
FIG.3A**FIG.3B**

FIG.4A**FIG.4B**

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FIG.5

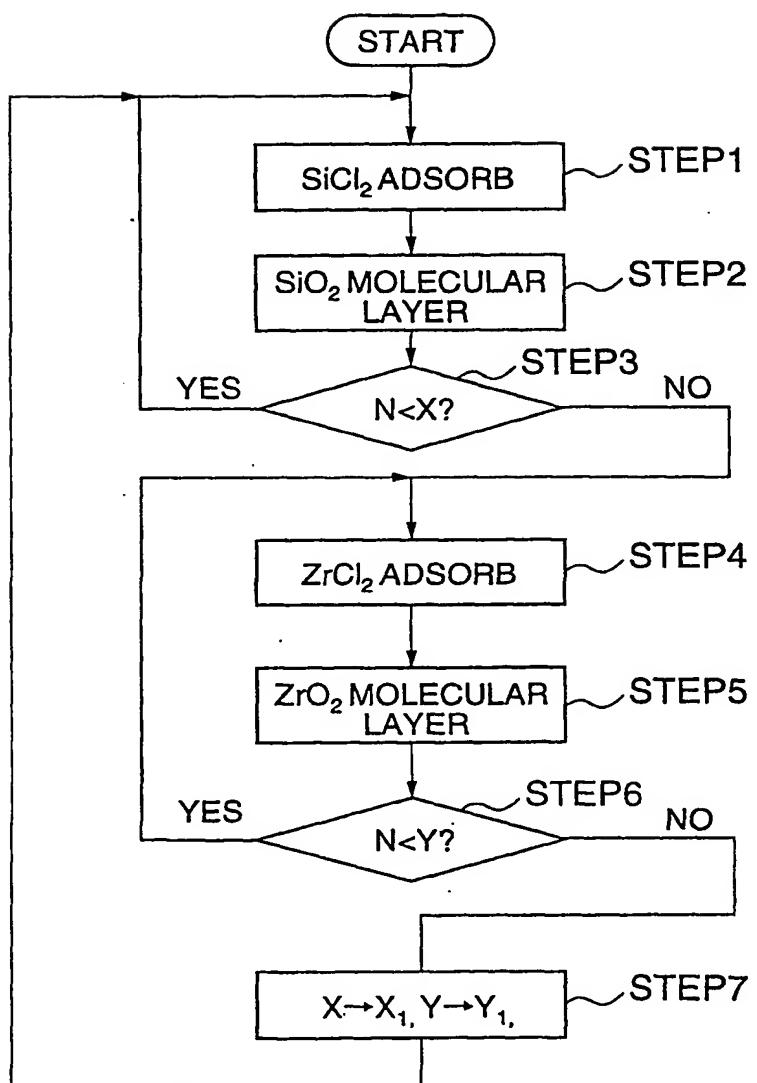
SOURCE	Ta(OC ₂ H ₅) ₅ 0.001~0.1torr 0.1~5mg/min 200~350°C	TaCl ₅ 0.01~0.1torr 0.1~5mg/min ↓	Zr(OC ₄ H ₉) ₄ 0.01~0.1torr 0.1~5mg/min ↓	ZrCl ₄ 0.01~0.1torr 0.1~5mg/min ↓	Al(OC ₃ H ₇) ₃ 0.01~0.1torr 0.1~5mg/min ↓	(CH ₃) ₃ Al 0.01~0.1torr 0.1~5mg/min ↓	SiCl ₄ 0.01~0.1torr 0.1~5mg/min ↓	Si(OC ₂ H ₅) ₄ 0.01~0.1torr 0.1~5mg/min ↓
ADSORB PROCESS	200~350°C, 10~0.001torr	↓	↓	↓	↓	↓	↓	↓
VACUUM GAS FLOWRATE TEMPERATURE	200~350°C, 10~0.001torr	↓	↓	↓	↓	↓	↓	↓
OXIDIZE PROCESS	H ₂ O NO ₂ O ₂ O ₃	200~350°C, 10~0.001torr 200~350°C, 10~0.001torr 300~400°C, 10~0.001torr 200~300°C, 10~0.001torr	↓	↓	↓	↓	↓	↓

FIG.6

CVD PROCESS	COMPOSITION TEMPERATURE SOURCE OXIDATION GAS	Ta_2O_5 400~600°C 0.1~10 torr $Ta(OC_2H_5)_5$ O_2	ZrO_2 $Zr(t-OC_4H_9)_4$ $t-OC_4H_9$	HfO_2 $H(C_5H_7O_2)_4$ $C_5H_7O_2$	SiO_2 $Si(OC_2H_5)_4$ OC_2H_5	Al_2O_3 $Al(I-OC_3H_7)_3$ $I-OC_3H_7$

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FIG.7



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FIG. 8

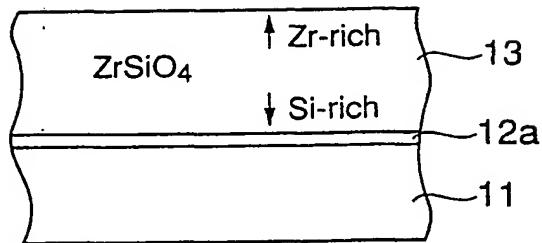


FIG. 9

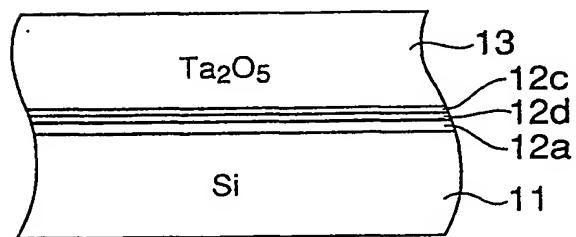
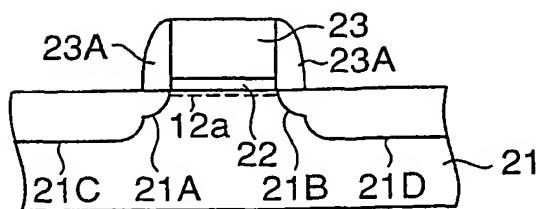


FIG. 10



INTERNATIONAL SEARCH REPORT

Intern'l Application No
PCT/JP 01/02262A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category ^o	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 020 243 A (WILK GLEN D ET AL) 1 February 2000 (2000-02-01)	21,23, 24,27-30
Y		1-5,7-9,
A	column 4, line 12 -column 7, line 55 table 1 ---	26 10
Y	GB 1 311 685 A (LICENTIA GMBH) 28 March 1973 (1973-03-28) the whole document figure 2 ---	1-5,7-9
Y	WO 99 39384 A (MICRON TECHNOLOGY INC) 5 August 1999 (1999-08-05) page 7, line 3 - line 11 page 9, line 13 -page 11, line 7 figure 1 ---	16,26 -/-

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Date of the actual completion of the International search

3 September 2001

Date of mailing of the International search report

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X	SATOSHI KAMIYAMA ET AL: "HIGHLY RELIABLE 2.5NM TA205 CAPACITOR PROCESS TECHNOLOGY FOR 256MBIT DRAMS" PROCEEDINGS OF THE INTERNATIONAL ELECTRON DEVICES MEETING. WASHINGTON, DEC. 8 - 11, 1991, NEW YORK, IEEE, US, 8 December 1991 (1991-12-08), pages 91-827-91-830, XP000347366 ISBN: 0-7803-0243-5	11,12
Y	the whole document ---	16-18
Y	LO G Q ET AL: "METAL-OXIDE-SEMICONDUCTOR CHARACTERISTICS OF CHEMICAL VAPOR DEPOSITED TA205 FILMS" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 60, no. 26, 29 June 1992 (1992-06-29), pages 3286-3288, XP000281268 ISSN: 0003-6951 the whole document ---	17,18
X	US 5 939 131 A (NAM KAB-JIN ET AL) 17 August 1999 (1999-08-17)	21,22,27
A	column 4, line 13 -column 5, line 8 ---	1,11,26
X	TREICHEL H ET AL: "LOW-PRESSURE CHEMICAL VAPOUR DEPOSITION OF TANTALUM PENTOXIDE FILMS FOR ULSI DEVICES USING TANTALUM PENTAETHOXIDE AS PRECURSOR" ADVANCED MATERIALS FOR OPTICS AND ELECTRONICS, WILEY AND SONS LTD, CHICHESTER, GB, vol. 1, no. 6, 1 December 1992 (1992-12-01), pages 299-308, XP000338535 ISSN: 1057-9257 the whole document ---	11,12, 21,22
X	CHIHIRO ISOBE ET AL: "EFFECT OF OZONE ANNEALING ON THE DIELECTRIC PROPERTIES OF TANTALUM OXIDE THIN FILMS GROWN BY CHEMICAL VAPOR DEPOSITION" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 56, no. 10, 5 March 1990 (1990-03-05), pages 907-909, XP000133481 ISSN: 0003-6951 the whole document ---	21,22
		-/-

INTERNATIONAL SEARCH REPORT

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PCT/JP 01/02262

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 02, 31 March 1995 (1995-03-31) & JP 06 310687 A (KAWASAKI STEEL CORP), 4 November 1994 (1994-11-04) abstract ---	1,6,7, 11,16, 21,26
A	US 5 837 593 A (KIM EUI-SONG ET AL) 17 November 1998 (1998-11-17) column 5, line 21 - line 38 ---	1,11,21
A	HITCHENS W R ET AL: "TANTALUM OXIDE THIN FILMS FOR DIELECTRIC APPLICATIONS BY LOW-PRESSURE CHEMICAL VAPOR DEPOSITION" JOURNAL OF THE ELECTROCHEMICAL SOCIETY, ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, US, vol. 140, no. 9, 1 September 1993 (1993-09-01), pages 2615-2621, XP000424115 ISSN: 0013-4651 the whole document ---	11,12
A	US 5 858 843 A (DOYLE BRIAN S ET AL) 12 January 1999 (1999-01-12) column 3, line 37 - line 60 column 6, line 12 - line 32 ---	1-30
A	LO G Q ET AL: "HIGHLY RELIABLE, HIGH-C DRAM STORAGE CAPACITORS WITH CVD TA205 FILMS ON RUGGED POLYSILICON" IEEE ELECTRON DEVICE LETTERS, IEEE INC. NEW YORK, US, vol. 14, no. 5, 1 May 1993 (1993-05-01), pages 216-218, XP000426253 ISSN: 0741-3106 the whole document -----	11,21
A	EP 0 641 027 A (OHMI TADAHIRO) 1 March 1995 (1995-03-01) the whole document -----	1-30

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat

ional Application No

PCT/JP 01/02262

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US 6020243	A 01-02-2000	JP 2000049349 A TW 402779 B US 6013553 A		18-02-2000 21-08-2000 11-01-2000
GB 1311685	A 28-03-1973	DE 1923279 A		23-12-1970
WO 9939384	A 05-08-1999	AU 2462199 A EP 1051744 A		16-08-1999 15-11-2000
US 5939131	A 17-08-1999	KR 207485 B JP 10074898 A TW 385514 B		15-07-1999 17-03-1998 21-03-2000
JP 06310687	A 04-11-1994	US 5521423 A		28-05-1996
US 5837593	A 17-11-1998	KR 183732 B JP 9121035 A US 6118146 A		20-03-1999 06-05-1997 12-09-2000
US 5858843	A 12-01-1999	NONE		
EP 0641027	A 01-03-1995	JP 5315608 A WO 9323878 A US 5528068 A		26-11-1993 25-11-1993 18-06-1996

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